

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
34	BRS	L35	31	park-joonbae.in.	US- PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:35	
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36	BRS	L37	1	35 and 36	US- PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:36	

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37	BRS	L38	4	kim-wonchan.in.	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:37	
38	BRS	L39	1	36 and 38	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:37	
39	BRS	L40	61	lee-kyeongho.in.	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:37	
40	BRS	L41	40	36 and "41"	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:38	
41	BRS	L42	1	36 and 40	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:39	
42	BRS	L43	0	jeong-dr-deog-kyoon.in.	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:38	

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43	BRS	L44	90	jeong-deog-kyoon.in.	US- PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:38	
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Day : Friday
Date: 11/4/2005

Time: 17:41:23



PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = PARK

First Name = JOONBAE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09442751	6731667	150	11/18/1999	ZERO-DELAY BUFFER CIRCUIT FOR A SPREAD SPECTRUM CLOCK SYSTEM AND METHOD THEREFOR	PARK, JOONBAE
09705696	Not Issued	71	11/06/2000	Automatic gain control loop apparatus	PARK, JOONBAE
09709637	6483355	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	PARK, JOONBAE
09940637	6498927	150	08/29/2001	AUTOMATIC GAIN CONTROL METHOD FOR HIGHLY INTEGRATED COMMUNICATION RECEIVER	PARK, JOONBAE
09940806	6424222	150	08/29/2001	VARIABLE GAIN LOW-NOISE AMPLIFIER FOR A WIRELESS TERMINAL	PARK, JOONBAE
09940807	6553089	150	08/29/2001	FRACTIONAL-N FREQUENCY SYNTHESIZER WITH FRACTIONAL COMPENSATION METHOD	PARK, JOONBAE
09940808	6704383	150	08/29/2001	SAMPLE AND HOLD TYPE FRACTIONAL-N FREQUENCY SYNTHESIZER	PARK, JOONBAE
10196136	6657498	150	07/17/2002	VARIABLE GAIN LOW-NOISE AMPLIFIER FOR A WIRELESS TERMINAL	PARK, JOONBAE
10207986	6850748	150	07/31/2002	RF FRONT END WITH REDUCED CARRIER LEAKAGE	PARK, JOONBAE
10229267	Not Issued	93	08/28/2002	ADAPTIVE LINEARIZATION TECHNIQUE FOR COMMUNICATION BUILDING BLOCK	PARK, JOONBAE
10231312	Not	93	08/30/2002	ZERO-DELAY BUFFER CIRCUIT	PARK, JOONBAE

	Issued			FOR A SPREAD SPECTRUM CLOCK SYSTEM AND METHOD THEREFOR	
<u>10253534</u>	6781424	150	09/25/2002	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	PARK, JOONBAE
<u>10284342</u>	6963620	150	10/31/2002	COMMUNICATION TRANSMITTER USING OFFSET PHASE-LOCKED-LOOP	PARK, JOONBAE
<u>10443835</u>	6876266	150	05/23/2003	LC OSCILLATOR WITH WIDE TUNING RANGE AND LOW PHASE NOISE	PARK, JOONBAE
<u>10689932</u>	Not Issued	20	10/22/2003	Radio receiver and method for AM suppression and DC-offset removal	PARK, JOONBAE
<u>10689986</u>	6952125	150	10/22/2003	SYSTEM AND METHOD FOR SUPPRESSING NOISE IN A PHASE-LOCKED LOOP CIRCUIT	PARK, JOONBAE
<u>10927012</u>	Not Issued	71	08/27/2004	Integrated circuit package having an inductance loop formed from a multi-loop configuration	PARK, JOONBAE
<u>10927013</u>	Not Issued	93	08/27/2004	SYSTEM AND METHOD FOR FILTERING SIGNALS IN A TRANSCIVER	PARK, JOONBAE
<u>10927014</u>	Not Issued	41	08/27/2004	Integrated circuit package having inductance loop formed from same- pin-to-same-bonding-pad structure	PARK, JOONBAE
<u>10927152</u>	Not Issued	41	08/27/2004	Integrated circuit package having inductance loop formed from a bridge interconnect	PARK, JOONBAE
<u>11057414</u>	Not Issued	20	02/15/2005	System and method for tuning a frequency generator using an LC oscillator	PARK, JOONBAE
<u>11066546</u>	Not Issued	30	02/28/2005	Highly linear variable gain amplifier	PARK, JOONBAE
<u>11227439</u>	Not Issued	19	09/16/2005	Apparatus and method of oscillating wideband frequency	PARK, JOONBAE
<u>11227909</u>	Not Issued	20	09/16/2005	Sigma-delta based phase lock loop	PARK, JOONBAE
<u>60164874</u>	Not Issued	159	11/12/1999	RECEIVER	PARK, JOONBAE
<u>60276912</u>	Not Issued	159	03/20/2001	Sample and hold type fractional-N frequency synthesizer	PARK, JOONBAE
<u>60276927</u>	Not Issued	159	03/20/2001	Fractional-N frequency synthesizer with fractional compensation	PARK, JOONBAE

				method	
<u>60279126</u>	Not Issued	159	03/28/2001	Automatic gain control method for highly integrated communication receiver	PARK, JOONBAE
<u>60279451</u>	Not Issued	159	03/29/2001	Apparatus and method of gain control for a preamplifier and a (tunable) low-noise amplifier in a wireless terminal	PARK, JOONBAE
<u>60315367</u>	Not Issued	159	08/29/2001	Adaptive linearization technique for communication building block	PARK, JOONBAE
<u>60386741</u>	Not Issued	159	06/10/2002	LC oscillator with wide tuning range and low phase noise	PARK, JOONBAE
<u>60421052</u>	Not Issued	159	10/25/2002	Gain-control sequence and associated DC offset cancellation method in a direct-conversion radio receiver	PARK, JOONBAE
<u>60421053</u>	Not Issued	159	10/25/2002	Radio receiver for AM suppression and DC-offset removal	PARK, JOONBAE
<u>60421054</u>	Not Issued	159	10/25/2002	Phase-locked-loop with fine resolution and wide-loop bandwidth	PARK, JOONBAE
<u>60421059</u>	Not Issued	159	10/25/2002	RF front-end filtering for a direct-conversion radio receiver	PARK, JOONBAE
<u>60421060</u>	Not Issued	159	10/25/2002	Reference modulation architecture for a low spurious phase-locked loop circuit	PARK, JOONBAE
<u>60422499</u>	Not Issued	159	10/31/2002	Spread-spectrum clock generation with Sigma-Delta modulation	PARK, JOONBAE
<u>60422500</u>	Not Issued	159	10/31/2002	System and method for cancelling DC offset and controlling gain in a wireless communications system	PARK, JOONBAE
<u>60422501</u>	Not Issued	159	10/31/2002	Precise clock frequency generation with sigma-delta controlled phase-locked loop	PARK, JOONBAE
<u>60498353</u>	Not Issued	159	08/28/2003	Integrated circuit package having inductance loop formed from same-pin-to-same-bonding-pad structure	PARK, JOONBAE
<u>60498354</u>	Not Issued	159	08/28/2003	Integrated circuit package having an inductance loop formed from a multi-loop configuration	PARK, JOONBAE
<u>60498356</u>	Not Issued	159	08/28/2003	Integrated circuit package having inductance loop formed from a bridge interconnect	PARK, JOONBAE
<u>60498366</u>	Not Issued	159	08/28/2003	System and method for filtering signals in a transceiver	PARK, JOONBAE

60545933	Not Issued	159	02/20/2004	System and method for tuning a frequency generator using an LC oscillator	PARK, JOONBAE
60551788	Not Issued	159	03/11/2004	Highly linear variable gain amplifier	PARK, JOONBAE
60614402	Not Issued	159	09/30/2004	Sigma-delta based phase lock loop	PARK, JOONBAE

Inventor Search Completed: No Records to Display.

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Last Name	First Name
<input type="text" value="PARK"/>	<input type="text" value="JOONBAE"/>

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PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = KIM

First Name = WONCHAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>07773413</u>	Not Issued	166	10/09/1991	DYNAMIC RANDOM ACCESS MEMORY CELL	KIM, WONCHAN
<u>07974162</u>	Not Issued	161	11/10/1992	MULTIVALUE STORING METHOD AND MEMORY CELL CIRCUIT	KIM, WONCHAN
<u>08120192</u>	Not Issued	161	09/13/1993	DYNAMIC RANDOM ACCESS MEMORY CELL	KIM, WONCHAN
<u>08634190</u>	Not Issued	161	04/18/1996	METHOD FOR RECOGNIZING CHANGES BETWEEN PICTURES	KIM, WONCHAN
<u>09397240</u>	Not Issued	161	09/16/1999	SYSTEM AND METHOD FOR PROVIDING USER-DEPENDENT SETUP OF A TV	KIM, WONCHAN
<u>09705696</u>	Not Issued	71	11/06/2000	Automatic gain control loop apparatus	KIM, WONCHAN
<u>09709637</u>	<u>6483355</u>	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	KIM, WONCHAN
<u>10140394</u>	Not Issued	93	05/07/2002	APPARATUS AND METHOD FOR SENSING THE DEGREE AND TOUCH STRENGTH OF A HUMAN BODY ON A SENSOR	KIM, WONCHAN
<u>10253534</u>	<u>6781424</u>	150	09/25/2002	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	KIM, WONCHAN
<u>60164874</u>	Not Issued	159	11/12/1999	RECEIVER	KIM, WONCHAN

Inventor Search Completed: No Records to Display.

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Last Name	First Name	
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PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = LEE

First Name = KYEONGHO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>08539816</u>	<u>5999571</u>	150	10/05/1995	TRANSITION-CONTROLLED DIGITAL ENCODING AND SIGNAL TRANSMISSION SYSTEM	LEE, KYEONGHO
<u>08622810</u>	<u>5825824</u>	150	03/27/1996	TRANSITION-CONTROLLED DIGITAL ENCODING AND SIGNAL TRANSMISSION SYSTEM	LEE, KYEONGHO
<u>08631420</u>	<u>5815041</u>	150	04/12/1996	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	LEE, KYEONGHO
<u>08646450</u>	<u>5905769</u>	150	05/07/1996	SYSTEM AND METHOD FOR HIGH-SPEED SKEW-INSENSITIVE MULTI-CHANNEL DATA TRANSMISSION	LEE, KYEONGHO
<u>08723694</u>	<u>5974464</u>	150	09/30/1996	SYSTEM FOR HIGH SPEED SERIAL VIDEO SIGNAL TRANSMISSION USING DC-BALANCED CODING	LEE, KYEONGHO
<u>09007707</u>	<u>5969552</u>	150	01/15/1998	DUAL LOOP DELAY-LOCKED LOOP	LEE, KYEONGHO
<u>09097021</u>	<u>6026124</u>	150	06/12/1998	TRANSITION-CONTROLLED DIGITAL ENCODING AND SIGNAL TRANSMISSION SYSTEM	LEE, KYEONGHO
<u>09098266</u>	<u>6157263</u>	150	06/16/1998	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP HAVING PHASE DETECTOR WITH DYNAMIC LOGIC STRUCTURE	LEE, KYEONGHO
<u>09121601</u>	<u>6335952</u>	150	07/24/1998	SINGLE CHIP CMOS	LEE, KYEONGHO

				TRANSMITTER/RECEIVER	
<u>09121863</u>	<u>6194947</u>	150	07/24/1998	VCO-MIXER STRUCTURE	LEE, KYEONGHO
<u>09298369</u>	<u>6374361</u>	150	04/22/1999	SKEW-INSENSITIVE LOW VOLTAGE DIFFERENTIAL RECEIVER	LEE, KYEONGHO
<u>09442751</u>	<u>6731667</u>	150	11/18/1999	ZERO-DELAY BUFFER CIRCUIT FOR A SPREAD SPECTRUM CLOCK SYSTEM AND METHOD THEREFOR	LEE, KYEONGHO
<u>09574571</u>	<u>6326826</u>	150	05/17/2000	Wide frequency-range delay-locked loop circuit	LEE, KYEONGHO
<u>09693516</u>	<u>6462624</u>	150	10/20/2000	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	LEE, KYEONGHO
<u>09705696</u>	Not Issued	71	11/06/2000	Automatic gain control loop apparatus	LEE, KYEONGHO
<u>09709310</u>	<u>6404277</u>	150	11/13/2000	GM-C TUNING CIRCUIT WITH FILTER CONFIGURATION	LEE, KYEONGHO
<u>09709311</u>	<u>6424192</u>	150	11/13/2000	PHASE LOCK LOOP (PLL) APPARATUS AND METHOD	LEE, KYEONGHO
<u>09709314</u>	<u>6754478</u>	150	11/13/2000	CMOS LOW NOISE AMPLIFIER	LEE, KYEONGHO
<u>09709315</u>	<u>6313688</u>	150	11/13/2000	Mixer structure and method for using same	LEE, KYEONGHO
<u>09709637</u>	<u>6483355</u>	150	11/13/2000	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	LEE, KYEONGHO
<u>09897975</u>	<u>6510185</u>	150	07/05/2001	SINGLE CHIP CMOS TRANSMITTER/RECEIVER	LEE, KYEONGHO
<u>09940637</u>	<u>6498927</u>	150	08/29/2001	AUTOMATIC GAIN CONTROL METHOD FOR HIGHLY INTEGRATED COMMUNICATION RECEIVER	LEE, KYEONGHO
<u>09940806</u>	<u>6424222</u>	150	08/29/2001	VARIABLE GAIN LOW-NOISE AMPLIFIER FOR A WIRELESS TERMINAL	LEE, KYEONGHO
<u>09940807</u>	<u>6553089</u>	150	08/29/2001	FRACTIONAL-N FREQUENCY SYNTHESIZER WITH FRACTIONAL COMPENSATION METHOD	LEE, KYEONGHO
<u>09940808</u>	<u>6704383</u>	150	08/29/2001	SAMPLE AND HOLD TYPE FRACTIONAL-N FREQUENCY SYNTHESIZER	LEE, KYEONGHO

<u>09985897</u>	<u>6512408</u>	150	11/06/2001	MIXER STRUCTURE AND METHOD FOR USING SAME	LEE, KYEONGHO
<u>10113600</u>	<u>6538498</u>	150	04/02/2002	GM-C TUNING CIRCUIT WITH FILTER CONFIGURATION	LEE, KYEONGHO
<u>10183974</u>	<u>6930560</u>	150	06/25/2002	HIGH-SPEED AND HIGH-PRECISION PHASE LOCKED LOOP	LEE, KYEONGHO
<u>10196136</u>	<u>6657498</u>	150	07/17/2002	VARIABLE GAIN LOW-NOISE AMPLIFIER FOR A WIRELESS TERMINAL	LEE, KYEONGHO
<u>10196479</u>	<u>6756828</u>	150	07/17/2002	PHASE LOCK LOOP (PLL) APPARATUS AND METHOD	LEE, KYEONGHO
<u>10207986</u>	<u>6850748</u>	150	07/31/2002	RF FRONT END WITH REDUCED CARRIER LEAKAGE	LEE, KYEONGHO
<u>10229267</u>	Not Issued	93	08/28/2002	ADAPTIVE LINEARIZATION TECHNIQUE FOR COMMUNICATION BUILDING BLOCK	LEE, KYEONGHO
<u>10231312</u>	Not Issued	93	08/30/2002	ZERO-DELAY BUFFER CIRCUIT FOR A SPREAD SPECTRUM CLOCK SYSTEM AND METHOD THEREFOR	LEE, KYEONGHO
<u>10253534</u>	<u>6781424</u>	150	09/25/2002	SINGLE CHIP CMOS TRANSMITTER/RECEIVER AND METHOD OF USING SAME	LEE, KYEONGHO
<u>10284342</u>	<u>6963620</u>	150	10/31/2002	COMMUNICATION TRANSMITTER USING OFFSET PHASE-LOCKED-LOOP	LEE, KYEONGHO
<u>10443835</u>	<u>6876266</u>	150	05/23/2003	LC OSCILLATOR WITH WIDE TUNING RANGE AND LOW PHASE NOISE	LEE, KYEONGHO
<u>10689932</u>	Not Issued	20	10/22/2003	Radio receiver and method for AM suppression and DC-offset removal	LEE, KYEONGHO
<u>10689986</u>	<u>6952125</u>	150	10/22/2003	SYSTEM AND METHOD FOR SUPPRESSING NOISE IN A PHASE-LOCKED LOOP CIRCUIT	LEE, KYEONGHO
<u>10690629</u>	Not Issued	30	10/23/2003	Bidirectional turbo ISI canceller-based DSSS receiver for high-speed wireless LAN	LEE, KYEONGHO
<u>10927012</u>	Not Issued	71	08/27/2004	Integrated circuit package having an inductance loop formed from a multi-loop configuration	LEE, KYEONGHO

10927013	Not Issued	93	08/27/2004	SYSTEM AND METHOD FOR FILTERING SIGNALS IN A TRANSCEIVER	LEE, KYEONGHO
10927014	Not Issued	41	08/27/2004	Integrated circuit package having inductance loop formed from same-pin-to-same-bonding-pad structure	LEE, KYEONGHO
10927152	Not Issued	41	08/27/2004	Integrated circuit package having inductance loop formed from a bridge interconnect	LEE, KYEONGHO
11057414	Not Issued	20	02/15/2005	System and method for tuning a frequency generator using an LC oscillator	LEE, KYEONGHO
11066546	Not Issued	30	02/28/2005	Highly linear variable gain amplifier	LEE, KYEONGHO
11227439	Not Issued	19	09/16/2005	Apparatus and method of oscillating wideband frequency	LEE, KYEONGHO
11227909	Not Issued	20	09/16/2005	Sigma-delta based phase lock loop	LEE, KYEONGHO
60004907	Not Issued	159	10/06/1995	HIGH-SPEED DIGITAL VIDEO SIGNAL TRANSMISSION SYSTEM	LEE, KYEONGHO
60082959	Not Issued	159	04/23/1998	SKEW-INSENSITIVE LVDS (LOW VOLTAGE DIFFERENTIAL SWING) RECEIVER	LEE, KYEONGHO
60136640	Not Issued	159	05/27/1999	UNLIMITED FREQUENCY RANGE DELAY-LOCKED LOOP CIRCUIT	LEE, KYEONGHO

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Inventor Name Search Result

Your Search was:

Last Name = JEONG

First Name = DR DEOG-KYOON

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09705696	Not Issued	71	11/06/2000	Automatic gain control loop apparatus	JEONG, DR DEOG- KYOON

Inventor Search Completed: No Records to Display.

Search Another: Inventor

Last Name	First Name
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10		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
11	BRS	L11	77	(plural\$3 near3 vga\$1 or variable adj2 gain\$1 near3 plural\$3 or variable adj2 amplif\$9 near3 plural\$3 or multi\$3 near3 vga\$1 or cascad\$3 near3 vga\$1 or variable adj2 gain\$1 near3 cascad\$3 or variable adj2 amplif\$9 near3 cascad\$3 or variable adj2 gain\$1 near3 multi\$3 or variable adj2 amplif\$9 near3 multi\$3 or bank\$1 near3 vga\$1 or serially near3 vga\$1 or series near3 vga\$1 or variable adj2 gain\$1 near3 serial\$4 or variable adj2 gain\$1 near3 series) same (AGC\$1)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 16:52	

	Error Definition	Err ors
11		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
12	BRS	L12	67	(plural\$3 near3 vagc\$1 or variable adj2 gain\$1 near3 plural\$3 or variable adj2 amplif\$9 near3 plural\$3 or multi\$3 near3 vagc\$1 or cascad\$3 near3 vagc\$1 or variable adj2 gain\$1 near3 cascad\$3 or variable adj2 amplif\$9 near3 cascad\$3 or variable adj2 gain\$1 near3 multi\$3 or variable adj2 amplif\$9 near3 multi\$3 or bank\$1 near3 vagc\$1 or serially near3 vagc\$1 or series near3 vagc\$1 or variable adj2 gain\$1 near3 serial\$4 or variable adj2 gain\$1 near3 series) same (AGC\$1)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 16:53	
13	BRS	L13	78	11 or 12	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 16:53	
14	BRS	L14	15	13 and (HPF or high adj2 pass)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 17:09	
15	BRS	L15	61	13 not (14 or 1 or 6 or 7)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 16:58	

	Error Definition	Err ors
12		
13		
14		
15		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
16	BRS	L16	2	("6420934").URPN.	USPAT	2005/11/04 16:59	
17	BRS	L17	3	("5841320" "6172559" "6205189").PN.	US-PGPUB USPAT ; USOCR	2005/11/04 17:00	
18	BRS	L18	0	15 and (HPF or HP or high adj2 pass)	US-PGPUB ; USPAT ; EPO; JPO	2005/11/04 17:09	

	Error Definition	Err ors
16		
17		
18		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
19	BRS	L19	36	(plural\$3 near3 vag\$1 or variable adj2 gain\$1 near3 plural\$3 or variable adj2 amplif\$9 near3 plural\$3 or multi\$3 near3 vag\$1 or cascad\$3 near3 vag\$1 or variable adj2 gain\$1 near3 cascad\$3 or variable adj2 amplif\$9 near3 cascad\$3 or variable adj2 gain\$1 near3 multi\$3 or variable adj2 amplif\$9 near3 multi\$3 or bank\$1 near3 vga\$1 or serially near3 vag\$1 or series near3 vag\$1 or variable adj2 gain\$1 near3 serial\$4 or variable adj2 gain\$1 near3 series) same (PLL\$1 or DLL\$1 or PDLL\$1 or phase adj2 lock\$3 adj2 loop\$1 or feedback near2 filter\$3 or loop near3 filter\$3 or loop near3 feedback)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 17:11	
20	BRS	L20	0	19 not 6	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 17:11	

	Error Definition	Err ors
19		
20		

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
21	BRS	L21	42	(vag\$1 or vag\$1 or vga\$1 or variable adj2 gain\$1 or variable adj3 amplif\$9 or gain\$1 adj2 stag\$3 near3 plural\$3 or gain\$1 adj3 stag\$3 near3 multi\$3 or first adj2 gain\$1 near3 second adj2 gain\$1) same (PLL\$1 or DLL\$1 or PDLL\$1 or phase adj2 lock\$3 adj2 loop\$1 or feedback near2 filter\$3 or loop near3 filter\$3 or loop near3 feedback) same (HPF of High adj2 pass)	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 17:21	
22	BRS	L22	1	"4990913".pn.	US- PGPUB ; USPAT ; EPO; JPO	2005/11/0 4 17:21	

	Error Definition	Err ors
21		
22		